

C1  
side walls formed on side surfaces of said first and second gates;

a protective layer formed on said field oxide, said protective layer being a material different than said field oxide;

B1  
an insulating layer formed on the substrate including said first and second gates, said side walls, said field oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole.

7. (Amended) The semiconductor device of claim 6, wherein said protective layer is a polysilicon layer.

B2  
9. (Amended) The semiconductor device of claim 6, wherein said first and second gates are MOSFET gates.

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Please add claims 11-15 as follows:

--11. A semiconductor device comprising:

S153  
a gate formed on an active region of a substrate;

a field oxide formed on the substrate adjacent the active region;

B7  
a protective layer formed on said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate including said gate, said field oxide

*Sub 13*  
and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole,

said protective layer being formed on said field oxide only.

12. The semiconductor device of claim 11, wherein said protective layer is a polysilicon layer.

*B3*  
*cont* 13. The semiconductor device of claim 11, wherein said gate is a MOSFET gate.

14. The semiconductor device of claim 11, further comprising side walls formed on side surfaces of said gate, said side walls being covered by said insulating layer.

15. The semiconductor device of claim 11, further comprising an additional gate formed on the substrate, said field oxide being formed on the substrate between said gate and said additional gate.